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EXAMINER	
DANIEL JR, WILLIE J	

ART UNIT	PAPER NUMBER
2617	

DATE MAILED: 11/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/991,749	TAKANO ET AL.	
	Examiner	Art Unit	
	Willie J. Daniel, Jr.	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to applicant's amendment filed on 29 August 2006. **Claims 1-3 and 5-10** are now pending in the present application. This office action is made **Final.**

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 5-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yanai** (**JP 05-046121 U**) (JPO Computer Translation; Thomson translation) in view of **Ogita** (**US 4,225,823**) and **Shiga et al.** (hereinafter Shiga) (**US 6,240,019 B1**).

Regarding **claim 1,** Yanai discloses an electronic tuning system comprising:

a voltage controlled oscillator (VCO 7) for generating a local frequency signal having a frequency according to a predetermined control voltage (see [0009]; Fig. 1);

a tuning circuit (2) which reads on the claimed "electronic tuner" coupled to the voltage controlled oscillator (7) for adjusting the predetermined control voltage to tune the local frequency signal to radio waves on an arbitrary channel in accordance with channel selection information (see [0009, 0006-0008, 0011-0012, 0014]; Fig. 1);

a DC-DC converter (13) which reads on the claimed "booster circuit" coupled to the voltage controlled oscillator (7) for boosting a source voltage to generate a boosted voltage in

order to ensure the predetermined control voltage (see [0009]; Fig. 1), where the DC-DC converter boost the supply voltage for operation; and

a memory (22) which read on the claimed "non-volatile memory" for storing the channel selection information (see [0009]; Fig. 1), where the frequency from the tuning or scanning is stored in memory. Yanai does not specifically disclose having the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage; in response to a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage was well known in the art, as taught by Ogita.

In the same field of endeavor, Ogita discloses the feature wherein the booster amplifier (79) which reads on the claimed "booster circuit" (see col. 6, lines 3-31; Fig. 5) includes,

a coil (76) coupled to a voltage source (+B) which reads on the claimed "power source" (see col. 6, lines 12-15; Fig. 5);

a switching element (81) coupled to the coil (76) for periodically conducting a DC current flowing through the coil to a ground to change the DC current (see col. 6, lines 12-18; Fig. 5);

a zener diode (89) coupled to the coil (76) for clamping an electromotive force induced in the coil (76) in accordance with a change in the DC current flowing through the coil (76) to a predetermined voltage (see col. 6, lines 12-31; Fig. 5), where the clamping of the EMF would be inherent; and

a capacitor (77) coupled to the zener diode (89) for smoothing the clamped voltage to generate a boosted voltage (see col. 6, lines 24-31; Fig. 5), where the signal flows through the capacitor in which smoothing of the voltage would be inherent .

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai and Ogita to have the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage, in order to provide an improved circuit capable of increasing S/N ratio, as taught by Ogita (see col. 1, lines 56-59). The combination of Yanai and Ogita does not specifically disclose features in response to a

predetermined write voltage wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the features in response to a predetermined write voltage wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage was well known in the art, as taught by Shiga.

In the same field of endeavor, Shiga discloses the feature in response to a predetermined write voltage wherein the boosted voltage of the booster circuit (7) is utilized as the predetermined write voltage (see abstract; col. 6, lines 23-40; col. 3, lines 12-15; col. 5, lines 30-35; Figs. 1 and 5), where the data is stored in a non-volatile memory (i.e., memory cell array 1) according to write voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, and Shiga to have the feature in response to a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage, in order to provide a non-volatile semiconductor memory device for sequentially selecting memory cells from a memory cell array to write data therein, as taught by Shiga (see col. 3, lines 11-17).

Regarding **claim 2**, the combination of Yanai, Ogita, and Shiga discloses every limitation claimed, as applied above (see claim 1), in addition Yanai further discloses the electronic tuning system according to claim 1, wherein the electronic tuner includes:

a frequency divider (i.e., programmable frequency divider circuit) coupled to the voltage controlled oscillator (7) for dividing the local frequency signal in accordance with a predetermined frequency division ratio to generate a divided local frequency signal (see [0009, 0011-0012, 0016]; Fig. 1);

a phase comparator (i.e., phase comparison circuit) coupled to the frequency divider (i.e., programmable frequency divider circuit) for comparing the frequency and phase of the divided local frequency signal with the frequency and phase of a reference frequency signal to generate a voltage signal proportional to the frequency difference and the phase difference (see [0009, 0006-0008; 0011-0014]; Fig. 1); and

a low-pass filter (12) coupled to the phase comparator for filtering a voltage signal to generate a filtered voltage signal, wherein the predetermined control voltage is generated by adding the boosted voltage to the voltage of the filtered voltage signal, and the channel selection information includes information on the predetermined frequency division ratio supplied to the frequency divider (see [0009, 0006-0008; 0011-0014]; Fig. 1).

Regarding **claim 5**, the combination of Yanai and Ogita discloses every limitation claimed as applied above (see claim 1). The combination of Yanai and Ogita does not specifically disclose having the feature of a voltage supply control circuit coupled to the booster circuit for supplying the boosted voltage to the non-volatile memory in response to a request for writing the channel selection information into the non-volatile memory. However, the examiner maintains that the feature a voltage supply control circuit coupled to the booster circuit for supplying the boosted voltage to the non-volatile memory in response to a request for writing the channel selection information into the non-volatile memory was well known in the art, as taught by Shiga.

Shiga further discloses feature a power supply control system (7) which reads on the claimed "voltage supply control circuit" coupled to the booster circuit (7) for supplying the boosted voltage to the non-volatile memory (1) in response to a request for writing the data

which reads on the claimed "channel selection information" into the non-volatile memory (1) (see abstract; col. 3, lines 12-15; col. 6, lines 23-40; Figs. 5, 27, 29A-B), where the booster circuit provides power supply control of the boosted voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, and Shiga to have the feature a voltage supply control circuit coupled to the booster circuit for supplying the boosted voltage to the non-volatile memory in response to a request for writing the channel selection information into the non-volatile memory, in order to provide a non-volatile semiconductor memory device for sequentially selecting memory cells from a memory cell array to write data therein, as taught by Shiga (see col. 3, lines 11-17).

Regarding **claim 6**, the combination of Yanai and Ogita discloses every limitation claimed as applied above (see claim 1). The combination of Yanai and Ogita does not specifically disclose having the feature wherein the non-volatile memory includes a flash memory which receives the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage. However, the examiner maintains that the feature wherein the non-volatile memory includes a flash memory which receives the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage was well known in the art, as taught by Shiga.

Shiga further discloses the feature wherein the non-volatile memory (1) includes a flash memory (1) which receives the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage (see abstract; col. 3, lines 12-15; col. 5, lines 30-35; col. 6, lines 23-40; Figs. 5, 9, 26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, and Shiga to have the feature wherein the non-volatile memory includes a flash memory which receives the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage, in order to provide a non-volatile semiconductor memory device for sequentially selecting memory cells from a memory cell array to write data therein, as taught by Shiga (see col. 3, lines 11-17).

Regarding **claim 7**, the combination of Yanai and Ogita discloses every limitation claimed as applied above (see claim 1). The combination of Yanai and Ogita does not specifically disclose having the feature wherein the non-volatile memory includes a voltage converter circuit coupled to the booster circuit for receiving the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage. However, the examiner maintains that the feature wherein the non-volatile memory includes a voltage converter circuit coupled to the booster circuit for receiving the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage was well known in the art, as taught by Shiga.

Shiga further discloses the feature wherein the non-volatile memory (1) includes a regulator (8) which reads on the claimed "voltage converter circuit" coupled to the booster circuit (7) for receiving the boosted voltage from the booster circuit (7) to generate an erasure voltage and a write voltage (see abstract; col. 3, lines 12-15; col. 5, lines 30-35; col. 6, lines 23-40; Figs. 5, 9, 26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, and Shiga to have the

feature wherein the non-volatile memory includes a voltage converter circuit coupled to the booster circuit for receiving the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage, in order to provide a non-volatile semiconductor memory device for sequentially selecting memory cells from a memory cell array to write data therein, as taught by Shiga (see col. 3, lines 11-17).

Regarding **claim 8**, the combination of Yanai and Ogita discloses every limitation claimed as applied above (see claim 7). The combination of Yanai and Ogita does not specifically disclose having the feature further comprising a voltage supply control circuit coupled between the booster circuit and the voltage converter circuit for supplying the boosted voltage to the voltage converter circuit in response to a request for writing the channel selection information into the non-volatile memory. However, the examiner maintains that the feature further comprising a voltage supply control circuit coupled between the booster circuit and the voltage converter circuit for supplying the boosted voltage to the voltage converter circuit in response to a request for writing the channel selection information into the non-volatile memory was well known in the art, as taught by Shiga.

Shiga further discloses the feature further comprising a voltage supply control circuit (7) coupled between the booster circuit (7) and the voltage converter circuit (8) for supplying the boosted voltage to the voltage converter circuit (8) in response to a request for writing the data which reads on the claimed "channel selection information" into the non-volatile memory (1) (see abstract; col. 3, lines 12-15; col. 5, lines 30-35; col. 6, lines 23-40; Figs. 5, 9, 26, 27, 29A-B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, and Shiga to have the feature further comprising a voltage supply control circuit coupled between the booster circuit and the voltage converter circuit for supplying the boosted voltage to the voltage converter circuit in response to a request for writing the channel selection information into the non-volatile memory, in order to provide a non-volatile semiconductor memory device for sequentially selecting memory cells from a memory cell array to write data therein, as taught by Shiga (see col. 3, lines 11-17).

Regarding **claim 9**, Yanai discloses a radio receiver (see Fig. 1) comprising:

a voltage controlled oscillator (7) for generating a local frequency signal having a frequency in accordance with a predetermined control voltage (see [0009]; Fig. 1);

a mixer (i.e., mixing/synthesizing circuit 8) coupled to the voltage controlled oscillator (7) for mixing a received signal with a local frequency signal to generate a mixed frequency signal (see [0009]; Fig. 1);

an intermediate frequency filter (i.e., intermediate frequency amplifying circuit 9) coupled to the mixer for filtering the mixed frequency signal to generate an intermediate frequency signal (see [0009]; Fig. 1);

a detector circuit (10) coupled to the intermediate frequency filter (i.e., intermediate frequency amplifying circuit 9) for demodulating the intermediate frequency signal to an audio signal (see [0009]; Fig. 1);

an electronic tuner (i.e., tuning circuit 2) coupled to the voltage controlled oscillator (7) for adjusting the predetermined control voltage to tune the local frequency signal to radio

waves on an arbitrary channel in accordance with channel selection information (see [0009, 0006-0008, 0011-0012, 0014]; Fig. 1);

a booster circuit (i.e., DC-DC converter 13) coupled to the voltage controlled oscillator (7) for boosting a source voltage to generate a boosted voltage in order to ensure a predetermined control voltage (see [0009]; Fig. 1), where the DC-DC converter boost the supply voltage for operation; and

a non-volatile memory (i.e., memory 22) for storing the channel selection information (see [0009]; Fig. 1), where the frequency is stored in memory from the tuning or scanning. Yanai does not specifically disclose having the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage; in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined

voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage was well known in the art, as taught by Ogita.

Ogita further discloses the feature wherein the booster amplifier (79) which reads on the claimed "booster circuit" (see col. 6, lines 3-31; Fig. 5) includes,

a coil (76) coupled to a voltage source (+B) which reads on the claimed "power source" (see col. 6, lines 12-15; Fig. 5);

a switching element (81) coupled to the coil (76) for periodically conducting a DC current flowing through the coil to a ground to change the DC current (see col. 6, lines 12-18; Fig. 5);

a zener diode (89) coupled to the coil (76) for clamping an electromotive force induced in the coil (76) in accordance with a change in the DC current flowing through the coil (76) to a predetermined voltage (see col. 6, lines 12-31; Fig. 5), where the clamping of the EMF would be inherent; and

a capacitor (77) coupled to the zener diode (89) for smoothing the clamped voltage to generate a boosted voltage (see col. 6, lines 24-31; Fig. 5), where the signal flows through the capacitor in which smoothing of the voltage would be inherent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of and Yanai and Ogita to have the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current

flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage, in order to provide an improved circuit capable of increasing S/N ratio, as taught by Ogita (see col. 1, lines 56-59). The combination of Yanai and Ogita does not specifically disclose having the feature in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the feature in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage was well known in the art, as taught by Shiga.

Shiga further discloses the feature in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit (7) is utilized as the predetermined write voltage (see abstract; col. 6, lines 23-40; col. 3, lines 12-15; col. 5, lines 30-35; Figs. 1 and 5), where the data is stored in a non-volatile memory (i.e., memory cell array 1) according to write voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, and Shiga to have the feature in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage, in order to provide a non-volatile semiconductor memory device for sequentially selecting memory cells from a memory cell array to write data therein, as taught by Shiga (see col. 3, lines 11-17).

Regarding **claim 10**, the combination of Yanai, Ogita, and Shiga discloses every limitation claimed, as applied above (see claim 9), in addition Yanai further discloses the radio receiver according to claim 9, wherein the electronic tuner includes:

a frequency divider (i.e., programmable frequency divider circuit) coupled to the voltage controlled oscillator (7) for dividing the local frequency signal in accordance with a predetermined frequency division ratio to generate a divided local frequency signal (see [0009, 0011-0012, 0016]; Fig. 1);

a phase comparator (i.e., phase comparison circuit) coupled to the frequency divider (i.e., programmable frequency divider circuit) for comparing the frequency and phase of the divided local frequency signal with the frequency and phase of a reference frequency signal to generate a voltage signal proportional to the frequency difference and the phase difference (see [0009, 0006-0008; 0011-0014]; Fig. 1); and

a low-pass filter (12) coupled to the phase comparator for filtering a voltage signal to generate a filtered voltage signal, wherein the predetermined control voltage is generated by adding the boosted voltage to the voltage of the filtered voltage signal, and the channel selection information includes information on the predetermined frequency division ratio supplied to the frequency divider (see [0009, 0006-0008; 0011-0014]; Fig. 1).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yanai (JP 05-046121 U)** (JPO Computer Translation; Thomson translation) in view of **Ogita (US 4,225,823)** and **Shiga et al.** (hereinafter Shiga) **(US 6,240,019 B1)** as applied to claim 2 above, and further in view of **Yanagibori (US 4,919,640)**.

Regarding **claim 3**, the combination of Yanai, Ogita, and Shiga discloses every limitation claimed, as applied above (see claim 2), in addition Yanai further discloses the feature a voltage control oscillator (7) (see [0009]; Fig. 1), where the radio set has VCO (7) for tuning and/or scanning functions. The combination of Yanai, Ogita, and Shiga does not specifically disclose having the feature wherein the voltage controlled oscillator includes: a varactor diode which varies its capacitance in response to the predetermined control voltage; and a local oscillator coupled to the varactor diode for generating a local frequency signal having a frequency in accordance with the capacitance of the varactor diode. However, the examiner maintains that the feature wherein the voltage controlled oscillator includes: a varactor diode which varies its capacitance in response to the predetermined control voltage; and a local oscillator coupled to the varactor diode for generating a local frequency signal having a frequency in accordance with the capacitance of the varactor diode was well known in the art, as taught by Yanagibori.

In the same field of endeavor, Yanagibori discloses the feature wherein the voltage controlled oscillator (VCO 141) includes:

a varactor diode (11D) which varies its capacitance in response to the predetermined control voltage (see col. 3, lines 61-67; col. 4, lines 11-36; Fig. 2); and

a local oscillator (14) coupled to the varactor diode for generating a local frequency signal having a frequency in accordance with the capacitance of the varactor diode (see col. 3, lines 61-67; col. 4, lines 11-36; Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, Shiga, and Yanagibori to have the feature wherein the voltage controlled oscillator includes: a varactor diode which varies its capacitance in response to the predetermined control voltage; and a local oscillator coupled to the varactor diode for generating a local frequency signal having a frequency in accordance with the capacitance of the varactor diode, in order to provide an auto tuning apparatus that can identify a correct tuning point, as taught by Yanagibori (see col. 2, lines 52-57).

Alternate **Claims 1** and **9** Rejections:

Claims 1 and **9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yanai (JP 05-046121 U)** (JPO Computer Translation; Thomson translation) in view of **Ogita (US 4,225,823)** and **Ryu (JP 06-203584 A)** (JPO Computer Translation; Thomson translation).

Regarding **claim 1**, Yanai discloses an electronic tuning system comprising:

a voltage controlled oscillator (VCO 7) for generating a local frequency signal having a frequency according to a predetermined control voltage (see [0009]; Fig. 1);

a tuning circuit (2) which reads on the claimed "electronic tuner" coupled to the voltage controlled oscillator (7) for adjusting the predetermined control voltage to tune the local

frequency signal to radio waves on an arbitrary channel in accordance with channel selection information (see [0009, 0006-0008, 0011-0012, 0014]; Fig. 1);

a DC-DC converter (13) which reads on the claimed "booster circuit" coupled to the voltage controlled oscillator (7) for boosting a source voltage to generate a boosted voltage in order to ensure the predetermined control voltage (see [0009]; Fig. 1), where the DC-DC converter boost the supply voltage for operation; and

a memory (22) which read on the claimed "non-volatile memory" for storing the channel selection information (see [0009]; Fig. 1), where the frequency from the tuning or scanning is stored in memory. Yanai does not specifically disclose having the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage; in response to a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a

predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage was well known in the art, as taught by Ogita.

In the same field of endeavor, Ogita discloses the feature wherein the booster amplifier (79) which reads on the claimed "booster circuit" (see col. 6, lines 3-31; Fig. 5) includes,

a coil (76) coupled to a voltage source (+B) which reads on the claimed "power source" (see col. 6, lines 12-15; Fig. 5);

a switching element (81) coupled to the coil (76) for periodically conducting a DC current flowing through the coil to a ground to change the DC current (see col. 6, lines 12-18; Fig. 5);

a zener diode (89) coupled to the coil (76) for clamping an electromotive force induced in the coil (76) in accordance with a change in the DC current flowing through the coil (76) to a predetermined voltage (see col. 6, lines 12-31; Fig. 5), where the clamping of the EMF would be inherent; and

a capacitor (77) coupled to the zener diode (89) for smoothing the clamped voltage to generate a boosted voltage (see col. 6, lines 24-31; Fig. 5), where the signal flows through the capacitor in which smoothing of the voltage would be inherent .

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai and Ogita to have the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an

electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage, in order to provide an improved circuit capable of increasing S/N ratio, as taught by Ogita (see col. 1, lines 56-59). The combination of Yanai and Ogita does not specifically disclose having the feature in response to a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the feature in response to a predetermined write voltage wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage was well known in the art, as taught by Ryu.

In the same field of endeavor, Ryu discloses the feature in response to a predetermined write voltage wherein the boosted voltage of the DC-DC converter (36) which reads on the claimed "booster circuit" is utilized as the predetermined write voltage (see abstract; [0013, 0018-0019, 0022-0024]; Fig. 1), where data is stored in a non-volatile semiconductor memory (EEPROM).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, and Ryu to have the features in response to a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage, in order to provide a non-volatile semiconductor memory that utilizes a single power supply for operation, as taught by Ryu (see abstract; [0010]).

Regarding **Claim 9**, Yanai discloses a radio receiver (see Fig. 1) comprising:

a voltage controlled oscillator (7) for generating a local frequency signal having a frequency in accordance with a predetermined control voltage (see [0009]; Fig. 1);

a mixer (i.e., mixing/synthesizing circuit 8) coupled to the voltage controlled oscillator (7) for mixing a received signal with a local frequency signal to generate a mixed frequency signal (see [0009]; Fig. 1);

an intermediate frequency filter (i.e., intermediate frequency amplifying circuit 9) coupled to the mixer for filtering the mixed frequency signal to generate an intermediate frequency signal (see [0009]; Fig. 1);

a detector circuit (10) coupled to the intermediate frequency filter (i.e., intermediate frequency amplifying circuit 9) for demodulating the intermediate frequency signal to an audio signal (see [0009]; Fig. 1);

an electronic tuner (i.e., tuning circuit 2) coupled to the voltage controlled oscillator (7) for adjusting the predetermined control voltage to tune the local frequency signal to radio waves on an arbitrary channel in accordance with channel selection information (see [0009, 0006-0008, 0011-0012, 0014]; Fig. 1);

a booster circuit (i.e., DC-DC converter 13) coupled to the voltage controlled oscillator (7) for boosting a source voltage to generate a boosted voltage in order to ensure a predetermined control voltage (see [0009]; Fig. 1), where the DC-DC converter boost the supply voltage for operation; and

a non-volatile memory (i.e., memory 22) for storing the channel selection information (see [0009]; Fig. 1), where the frequency from the tuning or scanning is stored in memory. Yanai does not specifically disclose having the features wherein the booster circuit includes,

a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage; in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage was well known in the art, as taught by Ogita.

In the same field of endeavor, Ogita discloses the feature wherein the booster amplifier (79) which reads on the claimed "booster circuit" (see col. 6, lines 3-31; Fig. 5) includes,

a coil (76) coupled to a voltage source (+B) which reads on the claimed "power source" (see col. 6, lines 12-15; Fig. 5);

a switching element (81) coupled to the coil (76) for periodically conducting a DC current flowing through the coil to a ground to change the DC current (see col. 6, lines 12-18; Fig. 5);

a zener diode (89) coupled to the coil (76) for clamping an electromotive force induced in the coil (76) in accordance with a change in the DC current flowing through the coil (76) to a predetermined voltage (see col. 6, lines 12-31; Fig. 5), where the clamping of the EMF would be inherent; and

a capacitor (77) coupled to the zener diode (89) for smoothing the clamped voltage to generate a boosted voltage (see col. 6, lines 24-31; Fig. 5), where the signal flows through the capacitor in which smoothing of the voltage would be inherent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai and Ogita to have the features wherein the booster circuit includes, a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage, in order to provide an improved circuit capable of increasing S/N ratio, as taught by Ogita (see col. 1, lines 56-59). The combination of Yanai and Ogita does not specifically disclose having the feature in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the feature in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage was well known in the art, as taught by Ryu.

Ryu further discloses the feature in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit (i.e., DC-DC converter 36) is utilized as the predetermined write voltage (see abstract; [0013, 0018-0019, 0022-0024]; Fig. 1), where data is stored in a non-volatile semiconductor memory (EEPROM).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanai, Ogita, and Ryu to have the features in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage, in order to provide a non-volatile semiconductor memory that utilizes a single power supply for operation, as taught by Ryu (see abstract; [0010]).

Response to Arguments

3. Applicant's arguments filed 29 August 2006 have been fully considered but they are not persuasive.

The Examiner respectfully disagrees with applicant's arguments as the applied reference(s) provide more than adequate support and to further clarify (see the above claims and comments in this section).

4. In addition to the previous JPO translations of **Yanai (JP 05-046121 U)** and **Ryu (JP 06-203584 A)**, Thomson English translations of the references are hereby supplied.

5. In response to applicant's argument on pg. 9, 3rd paragraph, "...none... discloses a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage...", the Examiner respectfully disagrees. The applicant admits on pg. 10 "...capacitor 77...is used as a filter for filtering an input signal...". The combination of Yanai and Shiga discloses a booster circuit as indicated in claim 1 above, in addition Ogita discloses a capacitor (77) coupled to the zener diode (89) for smoothing the clamped voltage to generate a boosted voltage (see col. 6, lines 24-31; col. 7, lines 6-11; Fig. 5), where the booster amplifier (79) provides a signal flow through the capacitor in which smoothing of the voltage would be inherent as evidenced by the fact that one of ordinary skill in the art would clearly recognize. The smoothing of the DC voltage/current is a common effect of a ripple filter or smoothing circuit.

6. Regarding applicant's comment on pg. 10, 3rd paragraph, "...it is possible to use the booster circuit as a circuit for providing a boosted voltage and a circuit for providing a write voltage...", the Examiner acknowledges comment. In addition, the practice of having

hardware components such as a booster circuit providing shared use or dual function is common and would have been easily conceived by one of ordinary skill in the art.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Willie J. Daniel, Jr. whose telephone number is (571) 272-7907. The examiner can normally be reached on 8:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WJD,JR/

WJD,JR
02 November 2006

ERIKA A. GARY
PRIMARY EXAMINER